SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING A HIGH POWER FACTOR SWITCHING PREREGULATOR WITH THE L6560/A TRANSITION MODE I.C.

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Active power factor correction techniques are going to grow in conversion applications. Market interest (legislation to be considered) is also moving towards fairly low (36-150W) conversion power ranges (lighting, monitor).
This paper describes an "easy to use" 8 Pin Controller that allows the realization of very low cost off-line Power Factor Correction.

Introduction

Conventional AC to DC converters employ a full wave rectifier bridge with a simple capacitor filter to draw DC power from the mains AC. This filter capacitor must be large enough to supply the total power during most of each half-cycle while instantaneous line voltage is below the DC output voltage. With this bulk capacitor filter, the line current waveform is a narrow pulse. Consequently the power factor is poor (0.5-0.6) due to high harmonic distortion of the current waveform.

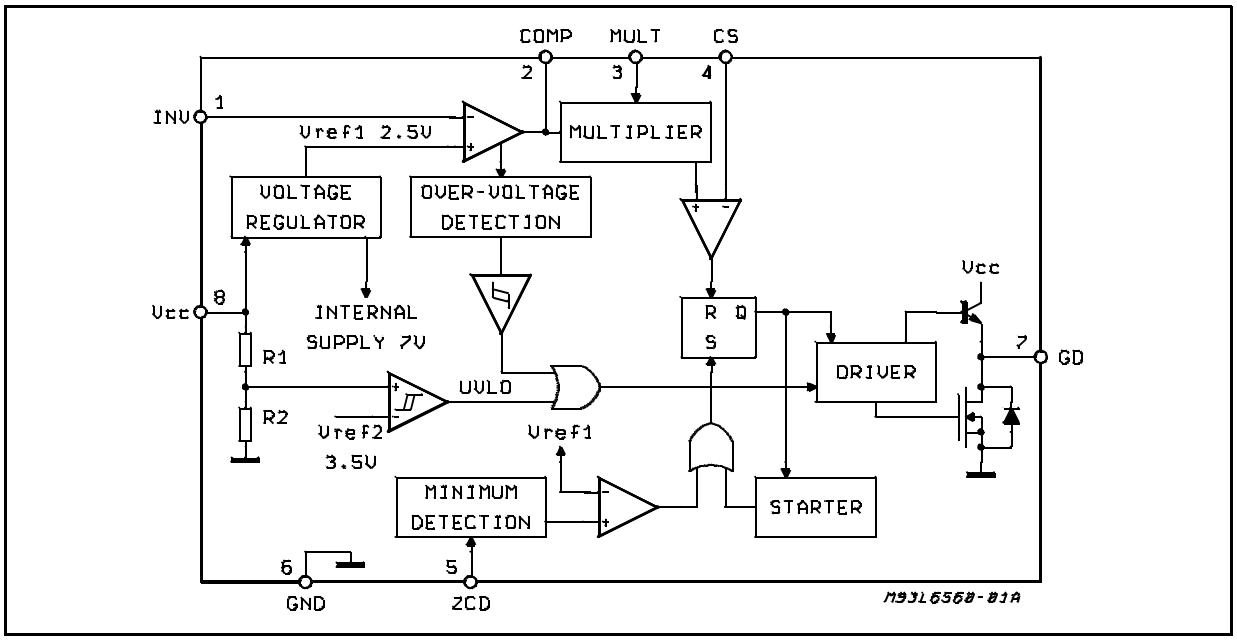
With a high power factor switching preregulator, interposed between the input rectifier bridge and the bulk filter capacitor, the power factor will be improved (up to 0.99). The current capability increased, the bulk capacitor peak current and the harmonic disturbances are reduced.

Switching at a frequency much higher than the line, the preregulator draws a half-sinusoidal input current, in phase with the line voltage. BOOST TOPOLOGY with its inductor at the input is well suited for PFC application. The input di/dt is low because the inductor is located between the bridge and the switch. This minimizes line noise and, in addition, the line spikes can be absorbed by the Boost Inductor.

L6560/A PFC controller Integrated Circuit

The L6560/A is an integrated circuit in Minidip and SO8 packages designed to perform the control of active power factor correction circuits. The I.C. is optimized for electronic ballast, but it can be easily used in switched mode AC-DC conversion. It can directly drive Mosfet or Igbt (see block diagram fig.1).

Figure 1: Block Diagram



The on chip features are:

- Undervoltage lockout with hysteresis and micropower start-up.
- Stable error amplifier.
- Output overvoltage protection.
- Transition Mode Operating
- Zero Current and coil Voltage detection.
- Internal start oscillator.

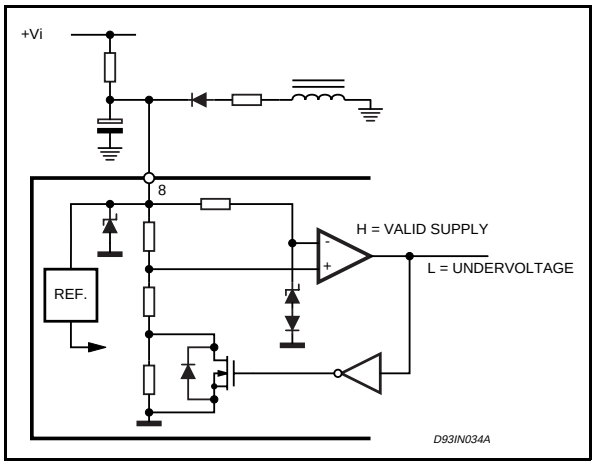
Device Blocks Description

Supply Block (see fig. 2):

A precise bandgap reference is internally built to ensure a good regulation.

The undervoltage comparator with hysteresis and the very-low supply current, before the turn-on threshold is reached, allows to minimize the start-up and supply circuitry.

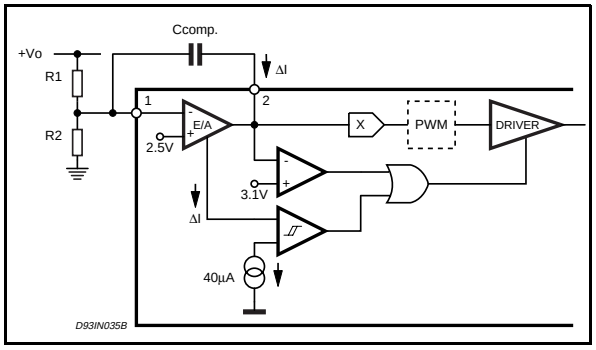
Figure 2: Supply Block Diagram



Error Amplifier and Overvoltage Detector Block (see fig. 3):

The Error Amplifier input, through the ratio of two external resistors connected to the output bus, allows the feedback for the boosted output DC voltage regulation. The E/A output will be connected to the compensation capacitor (see biasing of I.C.) to filter the twice rectified mains frequency (2f) so that the circuit doesn't attempt to regulate the output ripple.

Figure 3: Error Amplifier and Overvoltage Detector Block



The device is provided with an effective overvoltage protection (OVP), realized using the same input pin used for the DC voltage regulation. Since the compensation capacitor slows the E/A response, an internal fast OVP detector is implemented.

In steady state condition, the current through R1 is equal to the current in R2 because the comp. capacitor does not allow DC current (nor of course the inverting input of the E/A).

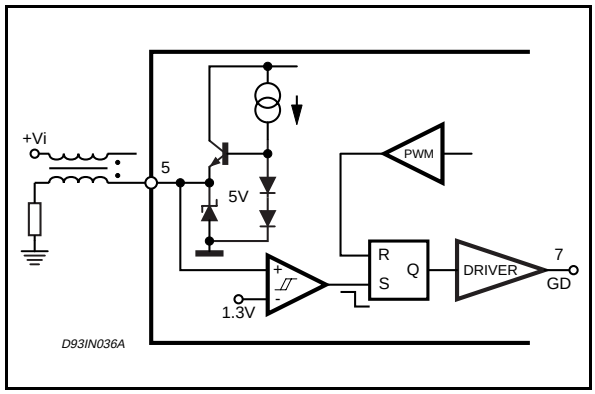
$$I_R = \frac{V_O - 2.5\ V}{R_1} = \frac{2.5\ V}{R_2}$$

When the output voltage increase, abruptly the current in R_1 will be increased of $\Delta V_{OUT}/R_1$ value and since the R_2 current is fixed by the internal 2.5V reference, the current must flow through the capacitor. This current is sensed inside the L6560/A I.C and compared with an internal 40 µA reference. If this limit is exceeded, the dinamic OVP is detected. As the time constant of this fast detection is over, in case the overvoltage condition persists (i.e. disconnected load), the output of the E/A goes below an internal reference and the OVP condition will be confirmed. The OVP detection disables the driver and the external Mosfet is forced off until the overvoltage condition disappears. Moreover, during the OVP conditions all the internal blocks are disabled (except the ZCD clamp) allowing to reduce the power consumption. The OVP limit ΔV_{OUT} will be selected by the equation:

$$\Delta V_{OUT} = R_1 \cdot 40\ \mu A$$

Zero Current Detection and Triggering Block (see fig. 4):

Figure 4: Zero Current Detection and Triggering Block



The zero current detection block switches on the external mosfet as the voltage acroos the boost inductor crosses zero (after the current through the boost diode is over).

This feature allows to reduce the equivalent drain capacitance energy, that is dissipated by the external Mosfet, because of the lower effective drain voltage at turn-on (V_{irms} instead of V_O).

To allow the start-up of the circuit without external parts, an internal pulser has been provided. The pulser, with repetition rate of 45 to 70 µs, forces the drive to deliver a narrow pulse (200 to 300ns) to the gate of the mosfet producing the signal for ZCD. On the other hand, for a correct working of the system, the switching frequency must be higher than 23kHz.

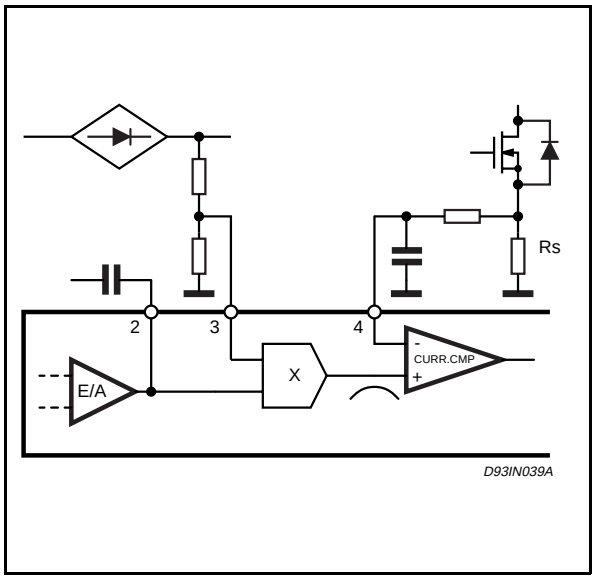
As the circuit is running, the signal for ZCD is obtained with an auxiliary winding of the booster inductor.

Multiplier Block (see fig. 5):

The multiplier delivers the programming signal to the current comparator. The error signal programs, cycle by cycle, the peak Mosfet current .

Current Comparator and PWM Latch (see fig.6):

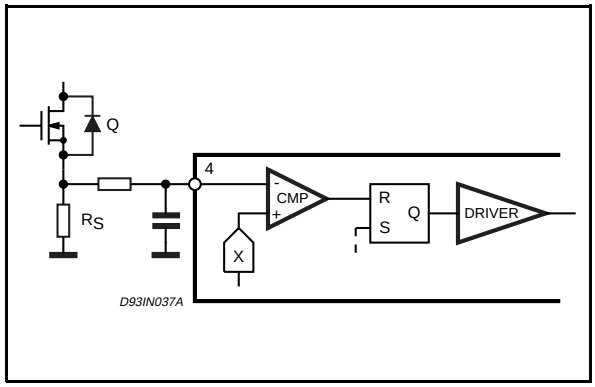
Figure 5: Multiplier Block Diagram



The current Comp. senses the voltage across the current sense resistor (R_S) and, comparing it with the programming signal delivered by the multiplier, produce the switching modulation.

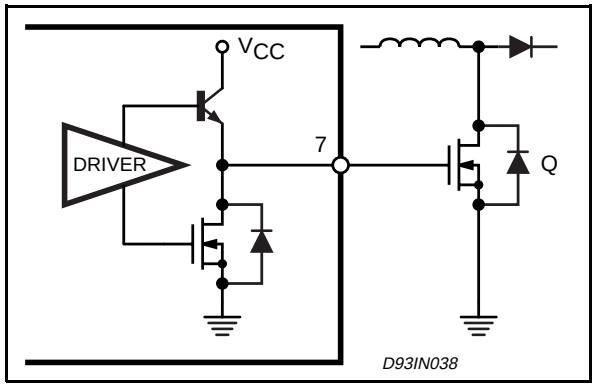
Driver (see fig.7):

Figure 6: Current Comparator and PWM Latch



A totem pole buffer, with 400mA, source and sink capability allows the external mosfet to switch at high frequency.

Figure 7: Driver



P.F.C. Boost Topology Operation

Although the easy-to-use I.C. and low external component count allows a simple approach, it can be useful to remind some design criteria.

The selection of the external components is mainly related on the application's parameters such as: Input main voltage range (V_{irms}), Output power(P_O), D.C. output voltage (V_O), Switching frequency (f_{sw}), etc.

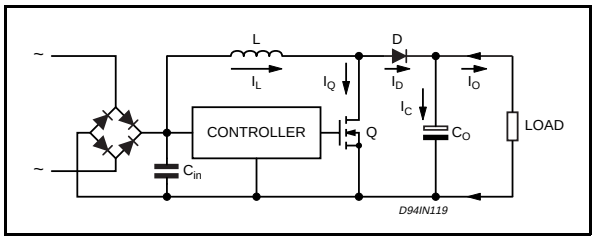
The operation of the P.F.C. transition mode controlled boost converter, can be summarized in the following description:

The A.C. mains voltage is rectified by a diodes bridge and the rectified voltage delivered to the boost converter. The boost converter section, using a switching technique, boosts the rectified input voltage to a D.C. controlled output voltage (V_O).

The section consists of a boost inductor (L), a controlled power switch (Q), a boost diode (D), an output capacitor (C_O) and, obviously, a control circuitry (see fig.8).

Since the input is a time-variable supply voltage

Figure 8: Boost Converter Circuit

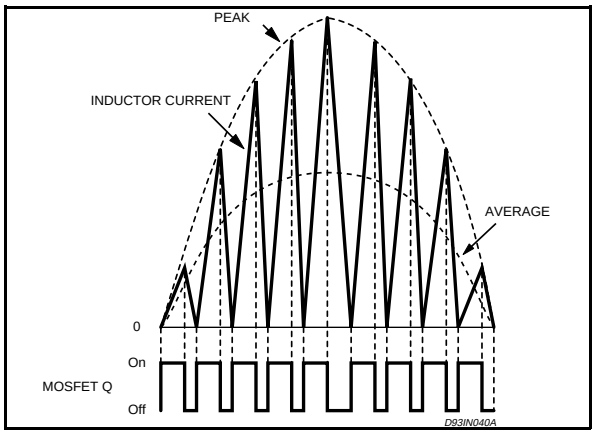


(sinewave), to make the input current shaped like the line voltage, the converter has to produce a boost inductor average current alike the rectified input voltage. To make it possible the I.C. L6560/A controls the system in transition mode.

Transition mode approch consists in a “zero current turn on” system, switching at variable frequency and duty cycle (see fig.9).

The signal on ZCD (pin 5) allows the Power Mos-

Figure 9: Current Wave



fet to be turned on after the boost inductor current is reduced to zero and the Mosfet drain capacitance is discharged to the rectified input voltage value (output of the bridge), instead of the output boosted D.C. voltage. Such a method will save crossover power dissipation at turn on.

Moreover, working in transition mode, allows to minimize the inductor size due to lower inductance value. On the other hand, higher current ripple on the inductor involves higher noise on the rectified main bus to be filtered with higher input capacitor values. This limits the use of the transition mode to lower power range applications than the continuous one.

Design Criterias

Here below some design criterias are described. For reference, the following definitions are useful:

V_{irms} = Effective A.C. mains voltage (spec. range)
V_o = Regulated output D.C. voltage (rated)
P_o = Output Power (rated)
P_i = Input Power
η = Efficiency (P_O/P_i)
I_{rms} = Effective A.C. mains current (P_L/V_{irms})

Power Section Design

INPUT BRIDGE

The input diodes bridge can be a standard off-line, slow_recovery, low cost device. The quantities to consider will be just the input current (I_{rms}) and the thermal data.

INPUT CAPACITOR

The input high frequency filter capacitor (Cin) has to attenuate the switching noise due to high frequency inductor current ripple (twice the average line value) see fig. 9.
The worst conditions will be found at the peak of the minimum rated input voltage.
The maximum high frequency voltage ripple ($r = \Delta V_I / V_I$) has to be imposed usually between 3% to 9%.

$$C_{in} = \frac{I_{rms}}{2\pi \cdot f_{sw} \cdot r \cdot V_{irms}}$$

where:
f_{sw} is the switching frequency

In real conditions the input capacitance will be designed taking into account the EMI filter.

OUTPUT CAPACITOR

The Output Capacitor Filter (C_O) choice depends on the electrical parameters that affect the filter performances and also on the final application.

The D.C. output voltage and overvoltage, the output power and voltage ripple are the first parameters to consider in all applications. The 100 ÷ 120 Hz (twice the mains frequency) voltage ripple (ΔV_O= 1/2 ripple peak/peak value) is a function of the capacitor impedence and the peak capacitor current ($I_{C(2f)pk}=I_O$).

$$\Delta V_O = I_O \cdot \sqrt{\frac{1}{(2\pi \cdot 2f \cdot C_O)^2} + ESR^2}$$

With a low ESR capacitor this can be simplyed:

$$C_O \geq \frac{I_O}{4\pi f \cdot \Delta V_O} = \frac{P_O}{4\pi f \cdot V_O \cdot \Delta V_O}$$

Although ESR normally does not affect the output ripple parameter, it has to be considered in power losses account both for the rectified main frequency and switching frequency.

The RMS capacitor ripple current

$$I_{C(2f)rms} = \frac{I_O}{\sqrt{2}}$$

If the application (e.g. computer supply) has to guarantee a specified Hold-Up time (t_{Hold}), the capacitance sizing criteria will change:

C_O has to deliver the supply energy for a certain time with a specified maximum dropout voltage.

$$C_O = \frac{2 \cdot P_O \cdot t_{Hold}}{V_{O\_min}^2 - V_{op\_min}^2}$$

where:

V_{O_min} is the minimum output voltage value (normally at the maximum load conditions)

V_{op_min} is the minimum output operative voltage before the 'power fail' detection.

BOOST INDUCTOR

Designing the Boost Inductor involves several parameters to be handled and different approaches can be used to define the quantities. The high voltage, flux density and freqency range, make the standard high frequency ferrite (gapped core-set) the most useful material in P.F.C. applications.

The inductance value (L) could be defined as follow (assuming $\eta = 1$):

$$P_O \approx \frac{L \cdot f_{sw} \cdot I_{Lpk}^2}{2 \cdot \delta}$$

$$L \approx \frac{2 \cdot P_O \cdot \delta}{I_{Lpk}^2 \cdot f_{sw}}$$

where:

δ (duty-cycle) = $1 - V_{it} / V_O$

I_{Lpk} is the peak inductor current

f_{sw} is the switching freq.

To be noted that δ and I_{Lpk} are variable with V_{in}:

$$\delta_{min} = \frac{V_O - \sqrt{2} \cdot V_{irms}}{V_O}$$

$$I_{Lpkmax} = 2\sqrt{2}\ \frac{P_O}{V_{irms}}$$

Being constant the ratio between the input voltage and current, the t_{on} of Power Mosfet is constant too. The switching frequency varies with the instantaneous (V_{in}) mains voltage. It has its minimum value at the maximum or the minimum mains voltage (depending on the V_{irms}/V_{oratio}). The inductor value is so defined by:

$$L \approx \frac{V_{irms}^2\ (V_O - \sqrt{2}\ V_{irms})}{2\ f_{sw\ (min)}\ P_O\ V_O}$$

Where Virms is the maximum or minimum mains voltage value depending on the one which produces the maximum inductor value.

Because of the internal oscillator characteristic (see ZCD and triggering block description), the minimum suggested switching frequency is fixed at about 23kHz.

The next step designing the Boost Inductor is the core choice. To get the approximated value of the minimum core size, the formula is:

$$Volume \geq 4 \cdot K \cdot L \cdot I_{rms}^2{}_{(max)}$$

where:

K = specific energy constant.
L = boost inductor values (in mH).

The constant K is a function of the magnetic path and for ferrite gapped core-sets depends on the ratio between the gap lenght (l_{gap}) and the total effective lenght (l_{eff}) of the magnetic core-set.

It has been found that K=1 is a good value to get the minimum core-set volume, in cm^3.

As the minimum size of the core-set is estimated, the suitable type will be selected with technical and economic considerations.

The next step in boost inductor design has to define the coil parameters. The number of turns and the wire section are important quantities to be defined.

The above mentioned formula:

$$P_O \approx \frac{L \cdot f_{sw} \cdot I_{Lpk}^2}{2 \cdot \delta}$$

referred to the magnetic path, can be rewritten as:

$$P_O \approx \frac{A_e \cdot l_{eff} \cdot H \cdot \Delta B \cdot f_{sw}}{2 \cdot \delta}$$

where:

A_e is the effective area of the core section.
l_{eff} is the effective magnetic path length
H is the magnetic field strength
ΔB is the deviated magnetic flux density.

To avoid the saturation of the core, related to the high permeability materials, it is necessary the use

of an air-gap in order to allow an adequate magnetic force range ($H+H_{gap}$). The ratio between the ferrite and the air path magnetic permeability, depends on the ferrite materials. Core materials for power application (i.e. B50/B51), have permeability value of about 2500 times the air one. This means that, using enough air-gap percentage lenght, it is possible to neglect the contribution of the magnetic reluctance of the core, using lgap instead of leff to semplify the calculation.

E.g. with 1% of air-gap length (that is the minimum suggested value) the introduced error, related to the neglected ferrite core magnetic field contribute, is about 4% .

The higher air-gap percentage, the lower the error percent.

The last formula can be written as:

$$P_O \approx \frac{A_e \cdot l_{gap} \cdot H_{gap} \cdot \Delta B \cdot f_{sw}}{2 \cdot \delta}$$

and simplified with

$$P_O \approx \frac{L \cdot f_{sw} \cdot I_{Lpk}^2}{2 \cdot \delta}$$

to obtain:

$$A_e \cdot l_{gap} \cdot H_{gap} \cdot \Delta B \approx L \cdot I_{Lpk}^2$$

because

$$l_{gap} \cdot H_{gap} \approx N \cdot I_{Lpk}$$

$$\Delta B = \mu_o \cdot \Delta H$$

we obtain:

$$N \approx \sqrt{\frac{L \cdot l_{gap}}{A_e \cdot \mu_o}}$$

where N is the number of turns of the coil.

As N is defined, it's recommended to check for the saturation of the core (rated $N \cdot I_{max}$ in the ferrites databook). If the check results too close to the rated limit, an increase of the l_{gap} (gap size) and a new calculus will be necessary.

The wire selection is oriented to limit the copper losses ($Pcu = 4/3\ I^2_{rms} \cdot Rcu$); due to the high frequency ripple the effective wire resistance is affected by skin and proximity effect. For this reason Litz wire or multi-wire solution is recommended. Finally, the available winding space will be evaluated, and if it isn't sufficient, a bigger core set will be considered.

An auxiliary winding, for the operation mode of the controller is necessary because the ZCD pin has to recognize when the voltage across the coil has gone to zero, it is a low cost thin wire coil and the number of turns is the only parameter to be defined; if the coil is used also for the I.C. supply, the voltage ratio defines the number of turns.

POWER MOSFET

The choice of the Mosfet mainly depends on the output power for its relation with R_{dson}. The breakdown voltage is just fixed by the output voltage, plus the overvoltage protection imposed limit and the safety margin.

The Mosfet power dissipation depends on two contributions:

Conduction losses:

$$P_{on} = I_{Qrms}^2 \cdot R_{DSon}$$

where:

$$I_{Qrms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{irms}}{9 \cdot \pi \cdot V_O}}$$

Switching losses: because of the operation mode (zero current turn_on) the crossover losses occur only at turn off of the mosfet:

$$P_{cross} = V_O \cdot I_{rms} \cdot t_{Fall} \cdot f_{sw}$$

where:

t_{Fall} is the crossover time at the turn off.

While at the turn on, the quantity to be considered is the capacitive loss:

$$P_{cap} = \frac{1}{2} \cdot C_d \cdot V_{Irms}^2 \cdot f_{sw}$$

Where C_d is the equivalent drain capacitance.

BOOSTER DIODE

The booster freewheeling diode is a fast recovery. The RMS diode current formula, useful for losses computation, is:

$$I_{Drms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{4\sqrt{2} \cdot V_{irms}}{9 \cdot \pi \cdot V_O}}$$

The breakdown voltage is fixed with the same criterias of the Mosfet.

L6560/A Controller Biasing Circuitry (pin by pin)

Referring to the schematic circuit of practical example shown below.

Pin 1(INV) leads to the inv. input of the error amplifier and to the overvoltage protection (OVP). A resistive divider will be connected between the regulated output voltage and INV pin. The typical voltage feedback input threshold is 2.5V and the precise overvoltage alarm level current is 40µA.

R7 and R8 will be selected as follow :

$$\frac{R7}{R8} = \frac{V_O}{2.5V} - 1$$

$$R7 = \frac{\Delta V_{OUT}}{40\ \mu A}$$

Pin 2(COMP) is the output of the error amplifier (and one of the two inputs to the multiplier). A feedback compensation network, placed between this pin and INV(1), reduces the frequency block gain to avoid the attempt of the system to control the output voltage ripple (100 ÷ 120Hz). Typically this compensation is just a capacitor that makes possible to reduce the gain for the low frequency output ripple (to minimize the third harmonic distortion) sustaining an high DC gain.

A simple criterion, to define the capacitor value, is to set the bandwidth (BW) from 20 to 30Hz.

$$BW = \frac{1}{2\pi \cdot R7 // R8 \cdot C_{comp}}$$

$$C_{comp} \geq \frac{1}{2 \cdot \pi \cdot R7 // R8 \cdot BW}$$

This pin can be used also to disable the IC. For this function see **Appendix A.**

Pin 3 (MULT) is the second multiplier input. It has to be connected, through a resistive divider, to the rectified mains. The feature of the multiplier is described by the relation:

$$V_{xcs} = k \cdot (V_{comp} - 3.5V) \cdot V_{mult}$$

where:

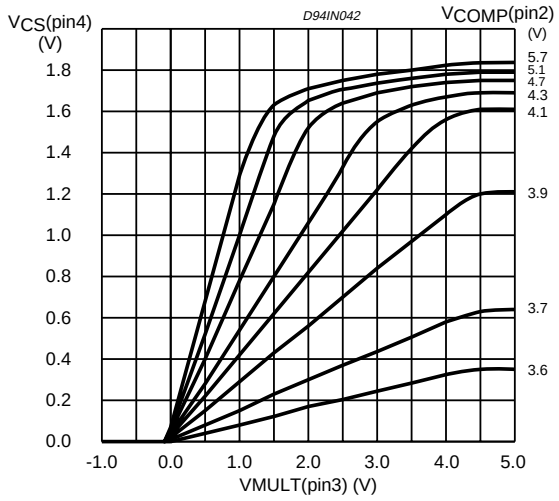
V_{XCS} (Mult.out) is the Input ref. to current-sense;

k is the multiplier gain;

V_{comp} is the Comp. output

V_{mult} is the multiplier input.

Figure 10: Multiplier characteristics family



In the application circuit:

$$V_{mult} = \frac{V_{in} \cdot R10}{R9 + R10}$$

$$V_{multpk} = \frac{V_{irms} \cdot \sqrt{2} \cdot R10}{R9 + R10}$$

The Mult. gain k can vary point to point. Fig.10 diagram shows the typical multiplier characteristics family in variable inputs condition. The output of the multiplier, controls the peak current flowing in the sense resistor, each cicle of operation.

Pin 4 (CS) is the input (inv.in) for the current sense comparator, the instantaneous Mosfet current is converted in a proportional voltage signal by an external sense resistor. Comparing this signal with the threshold set by the multiplier output, as the current exceed the set value, the power mosfet will be turned off by the reset signal until next set by the PWM latch. An internal circuit (Zerocurrent comparator) ensures that the PWM latch can't be set until the signal on pin 4 (CS) disappear.

The sense resistor (R_s) value is calculated as:

$$R_s \leq \frac{V_{xcspk}}{I_{Rspk}}$$

where: V_{xcspk} cannot exceed 1.6V max. value

$$I_{Rspk} = 2 \cdot \sqrt{2} \cdot P_i / V_{irms}$$

Pin 5 (ZCD) is the input to the zero current detector. The ZCD pin has to be connected, through a limiting resistor, to the auxiliary winding of the booster inductor. To perform the ZCD (zero-coil current and voltage) function the chip processes the inductor signal and turns on the external Mosfet as the voltage at the pin crosses the threshold level 2.3V to 1.1V (negative sensitive edge).

Pin 6 (GND), this pin is the common reference of the circuitry.

Pin 7 (GD), output of the driver, this pin is able to drive an external Mosfet with 400mA (source and sink).

Pin 8 (Vcc). Input for the supply voltage, this pin is externally connected to a filter capacitor. The minimum start up supply voltage has to be reached. (It depends on the version, see electrical characteristics on the datasheet).

If the supply decreases below V_{CCoff} the device recognizes the undervoltage condition and stops driving the external Mosfet.

PRACTICAL DESIGN EXAMPLE

To fix the main concepts, here below the demonstration board design criteria are described and the evaluation results are reported.

Demo 1: Target specifications

AC mains RMS voltage:	V_{Irms} = 88V to 132V
DC output regulated voltage:	V_O = 240V
Rated output power:	P_O = 100W
Full load output voltage ripple:	$\Delta V_O \leq \pm 10V$
Maximum output overvoltage:	ΔV_{OUT} = 60V

Demo 2: Target specifications

AC mains RMS voltage:	V_{Irms} = 176V to 264V
DC output regulated voltage:	V_O = 400V
Rated output power:	P_O = 120W
Full load output voltage ripple:	$\Delta V_O \leq \pm 15V$
Maximum output overvoltage:	ΔV_{OUT} = 40V

To match the above specifications the material selection, expecially for the most critical components, is an important step.

Power Mosfet (MOS):

Two parameters are useful to select the best device. The minimum blocking voltage ($V_{(BR)DSS}$) and the R_{DSON} because of power dissipation.

DEMO 1:

The selected device is the STP10NA40, because the $V_{(BR)DSS}$ = 400V is enough for the application and the $R_{DSON(25°C)} = 0.55\Omega$ ($R_{DSON(75°C)} = 0.7\Omega$) causes a ON-STATE power dissipation of:

$P_{ON} = I_{Qrms}^2 \cdot R_{DSON(75°C)} = 1.03 \cdot 0.7 = 740$ mW.

DEMO 2:

The selected device is the STP5NA50, because the $V_{(BR)DSS}$ = 500V is enough for the application and the $R_{DSON(25C)} = 1.6\Omega$ ($R_{DSON(75°C)} = 2\Omega$) causes a ON-STATE power dissipation of:

$P_{ON} = I_{Qrms}^2 \cdot R_{DSON(75°C)} = 0.29 \cdot 2 = 585$ mW.

Booster Diode (D1):

Fast recovery diode suitable for rated breakdown voltage are used on demoboards. The plastic axial package BYT03-400 and BYT13-600 has been selected.

Booster Inductor (T):

Inductor design starts defining the inductance value (L), considering the minimum frequency not less than 23kHz.

DEMO 1:

From the formula showed in the boost design section, the inductance value of about 0.6mH gives a minimum switching frequency of 28kHz. The magnetic core size estimate (Volume $\geq 4 \cdot K \cdot L \cdot I_{rms}^2{}_{(max)}$) results of 3.5cm^3 and so the ETD29 x 16 x 10 (effective volume of 5.4cm^3) has been selected.

DEMO 2:

The inductance value of about 0.8mH gives the minimum switching frequency of 24kHz. The same magnetic core ETD29 x 16 x 10 has been selected.

The other coil data are reported in the schematic diagram (figg.11 and 12). To reduce copper losses a multiwire solution (10 x 0.02mm) has been adopted. Measuring the series resistance (R_{CU}) at 25kHz results: 0.56Ω on DEMO1 and 0.7Ω on DEMO 2. The maximum copper losses are: $P_{CU} = I_{Lrms}^2 \cdot R_{CU}$ where $I_{Lrms} = 2/\sqrt{3}\ I_{rms}$. Considering a converter efficiency of 95% at the minimum mains voltage, follow: $P_{CU} = 1.9 \cdot 0.56 =$ 1.06W on DEMO 1, and $P_{CU} = 0.68 \cdot 0.7 =$ 0.48W.

Output Filter capacitor (C_O):

In this application the output voltage ripple is the parameter considered to select capacitance value.

DEMO 1:

The capacitance of 150µF and rated voltage 385V gives on output voltage ripple $\Delta V_O = \pm 4V$.

DEMO 2:

The capacitance of 47µF and rated voltage 450V gives an output voltage ripple $\Delta V_O = \pm 10V$.

Sense Resistor (R6):

The resistance value has been selected looking at the multiplier characteristic diagram (see fig.10), because both the sense resistance and the divider (R9,R10) define the working point of the system. The metallic film resistor are suited for high peak current flowing in this resistor.

The schematic circuit of applications of figg.11 and 12, report the values of all parts used.

Figure 11: Typical Application Circuit (100W, 110VAC)

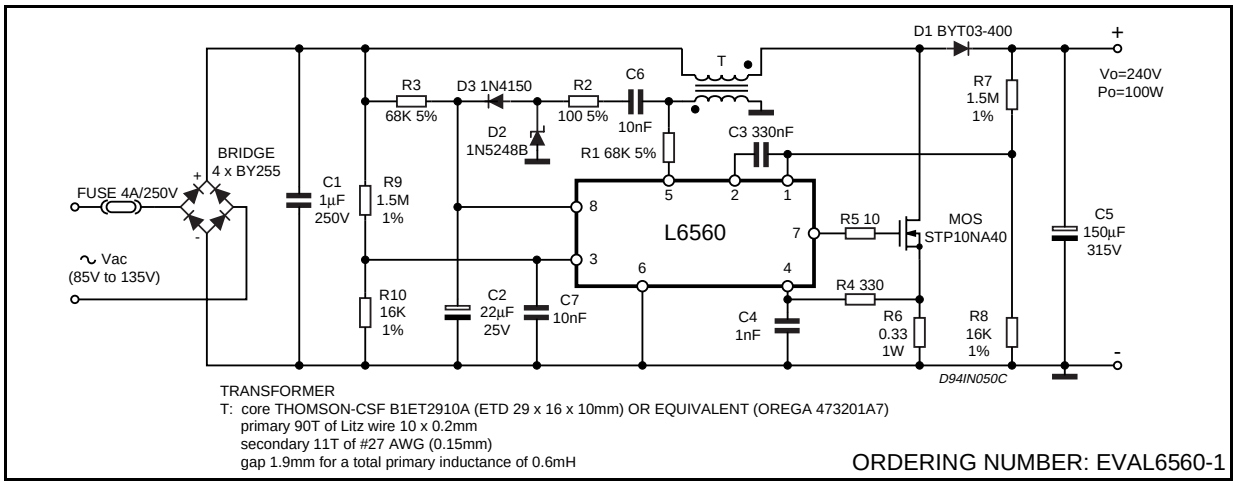


Figure 12: Typical Application Circuit (120W, 220VAC)

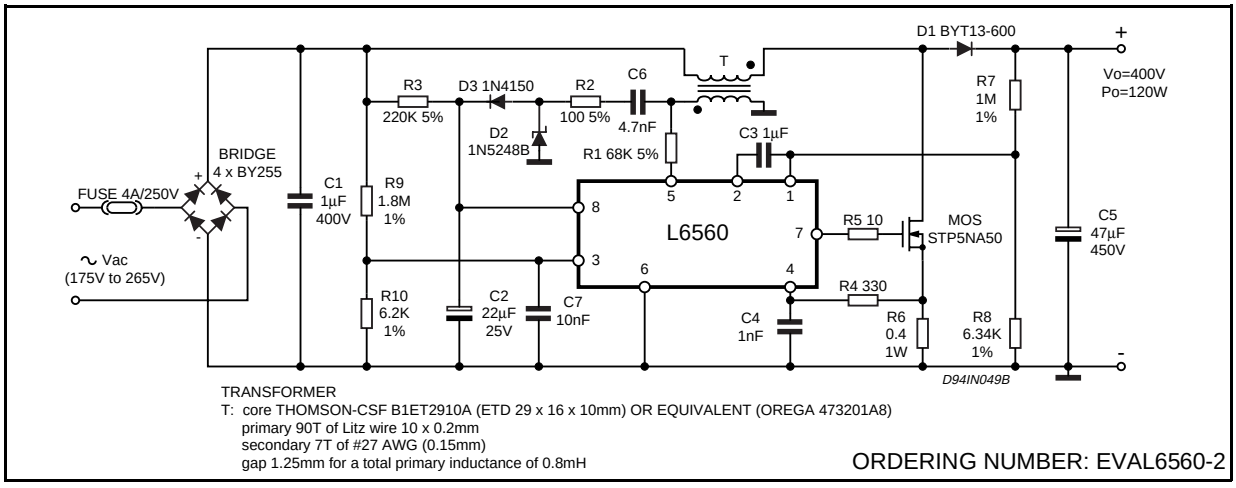
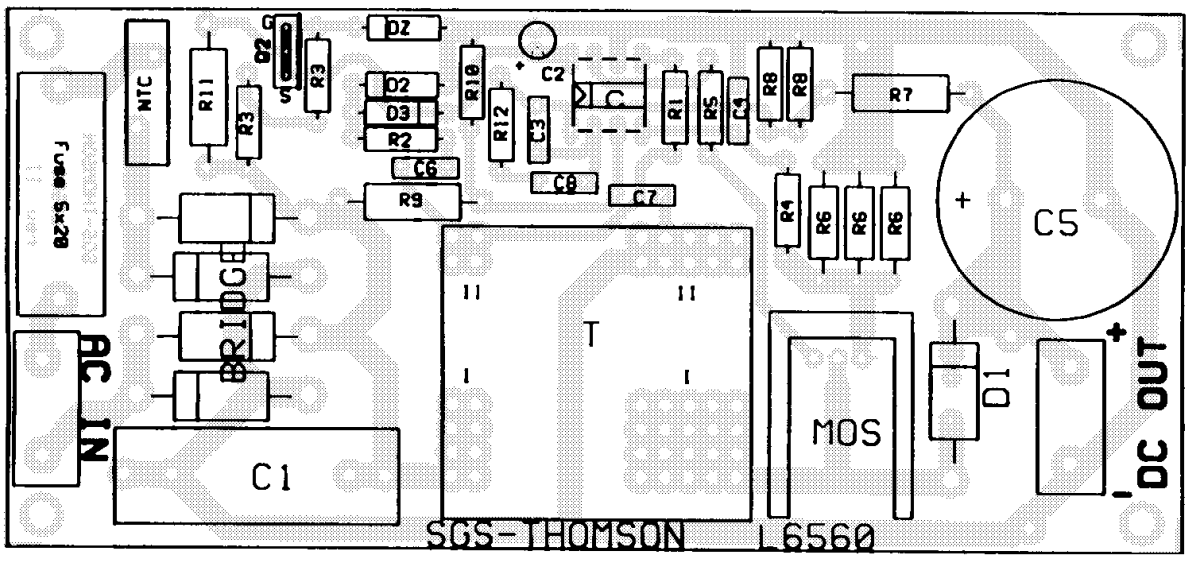
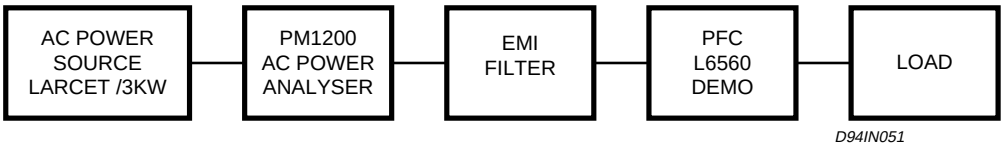


Figure 13: P.C. Board and component Layout of the Figg. 11 and 12 (1:1 scale)



DEMOBOARD EVALUATION RESULTS

To evaluate the PFC demoboard performances, the following parameters have been tested: PF(power factor), A_THD(percentage of current total harmonic distortion), H3..H9(percentage of current n^{th} harmonic amplitude), ΔV_O (output voltage ripple), V_O (output voltage), η (efficiency). Test configuration, equipment and results are shown below:.



DEMO 1:

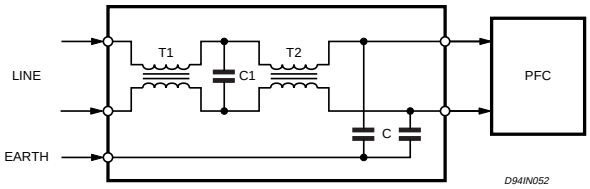
V_I	P_I	PF	A_THD	H3	H5	H7	H9	V_O	P_O	ΔV_O	η
[V_{rms}]	[W]		[%]	[%]	[%]	[%]	[%]	[V]	[W]	[V]	[%]
88	110.2	0.997	2.47	2.04	0.98	0.44	0.19	237.4	102.5	4	93.0
110	108.7	0.999	2.37	2.10	0.58	0.40	0.32	237.4	102.5	4	94.0
132	107.9	0.999	2.57	2.33	0.48	0.40	0.32	237.4	102.5	4	95.0

DEMO 2:

V_I	P_I	PF	A_THD	H3	H5	H7	H9	V_O	P_O	ΔV_O	η
[V_{rms}]	[W]		[%]	[%]	[%]	[%]	[%]	[V]	[W]	[V]	[%]
180	127.3	0.995	3.48	2.68	0.95	0.62	0.44	398.1	122.0	10	95.8
220	126.5	0.988	6.27	4.70	1.96	1.39	1.17	398.1	122.0	10	96.4
260	126.0	0.976	9.56	7.09	2.64	2.42	2.06	398.1	122.0	10	96.8

EMI/RFI filter

The harmonic content measurement has been done using an EMI/RFI filter interposed between the AC source and the demoboard under test, while the efficiency has been calculated without the filter contribution. The used filter is shown:



where:

T1 = 1mH
T2 = 27mH
C1 = 0.22µF, 630V
C = 2.2nF, 630V

Note

The PC board has been designed to accept some additional components, not used in this one. For example, The NTC resistor could be placed on on board to avoid in rush current risk. Since, normally, in evaluation stage this risk doesn't arise, the part has been shorted.

APPENDIX A

Disable

The PFC controller L6560 allows an easy mode to be disabled. If for some reason, the system using PFC section needs to disable this function, the best way is to force Pin2 (E/A output) to a voltage below 2.5V (see fig A1). That allows also to reduce the supply consumption of the IC during the disable so the startup circuit is able to restart the system once the disable condition is removed.

Figure A1.